White Paper

Flat Field Transistor (FFT) Technology

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Abstract: In this White Paper we present a detailed simulation study of the novel Flat Field Transistor (FFT) aiming to improve the performance, lower the leakage and reduce the statistical variability in 20nm and earlier bulk CMOS technology generations. In this device the implanted Source/Drain extensions and deep *p-n* junctions are replaced by epitaxially overgrown Source/Drain regions rising above the channel interface leading to superior electrostatic integrity. The FFT performance is highlighted in comparison with typical 20 nm bulk CMOS technology transistors. First, results illustrating the transistor performance improvement are presented. This is followed by a detailed study of the transistor variability and reliability. The corresponding improvement in the circuit performance is illustrated using ring oscillator (RO) and 6-T SRAM simulations.

1. Introduction

It is common wisdom that the conventional 'bulk' CMOS technology has reached the end of the road due to lack of performance [1] and intolerable statistical variability [2]. The saturation of the performance with scaling in bulk MOSFETs is deeply rooted into the way short channel effects are controlled by reducing the thickness of the depletion layer under the gate. A linear reduction of the depletion layer width, in parallel with scaling of the transistor dimensions, requires a quadratic increase in the channel doping concentration. As a result, channel doping in the range of 1×10^{19} cm^{-3} has become necessary to guarantee electrostatic integrity in a typical 20 nm CMOS technology transistor. The negative impact on performance due to the increase in the channel doping is twofold. First, the corresponding increase of the charge in the depletion layer under the gate increases the effective vertical electric field and reduces the channel mobility by sliding it to the right of the 'universal' mobility curve [3]. Second, at such high channel doping concentrations, the impurity scattering starts to play an important role and could further reduce the channel mobility below the corresponding surface roughness dominated 'universal' mobility. The effect is even stronger when the 'universal' mobility curve is elevated by strain [4]. Unfortunately, it is extremely difficult to counter-balance these negative effects by further scaling of the effective oxide thickness (EOT) [5], or by increasing the strain [6]. Both the channel doping and the high effective vertical electric field can be drastically reduced in FinFETs, as introduced by Intel in their the 22nm CMOS technology [7], and in fully depleted SOI (FDSOI) transistors introduced by ST in their 28nm CMOS technology [8] due to better electrostatic integrity marking the end of the bulk CMOS technology scaling. However, both FinFET and FDSOI CMOS technologies result in significant increase in the manufacturing costs compared to the bulk CMOS technology.

Still low cost, low power and high reliability bulk CMOS technology is desirable for the growing market of the 'install and forget' Internet of Things (IoT) applications and 'on chip' Artificial Intelligence (AI) applications. Unfortunately, the existing 60nm, 40nm, 28nm and 20nm bulk CMOS technologies cannot meet the IoT requirements in terms of power, leakage and reliability. In this white paper we present new Flat Field Transistor (FFT) bulk CMOS technology that dramatically improves the electrostatic integrity and reduces the short channel effect in comparison with the convention bulk MOSFETS simultaneously reducing the manufacturing costs by up to 5%. In the FFT, the implanted Source/Drain extensions and the deep *p-n* junctions are replaced by epitaxially overgrown Source/Drain regions that rise above the channel interface, which results in superior electrostatic integrity. This allows a dramatic reduction of the channel doping that has a twofold effect: Firstly, the reduced ionised impurity scattering in the channel improves the mobility and the corresponding drive current. Secondly, the decrease in the channel doping concentration dramatically reduces the statistical variability. Both the improved performance and the reduced statistical variability deliver significant reduction in the leakage current at equivalent drive current. The reduced channel doping and vertical and lateral electric

fields also reduce the negative bias temperature instability (NBTI) and hot carrier injection (HCI) degradations, thus improving the lifetime of the IoT and AI chips.

The FFT transistor design is presented in Section II. The drive current performance of the FFT is discussed in Section III. The statistical variability and reliability of the FFT is presented in section IV. Finally, the circuit performance of the FFT is presented in section V before the conclusions are drawn in Section VI.

2. Device Description

The concept of the *n*-channel FFT is illustrated in Fig. 1 in comparison with an equivalent 20 nm Bulk CMOS MOSFET. The two transistors have 25 nm physical channel length and 0.85 nm equivalent oxide thickness. In this paper we consider high-k/metal gate stack. The figures include the equipotential distribution, indicated also are the extension of the depletion layer and the corresponding field lines. The simulations are carried out with the drift-diffusion (DD) module of the Synopsys 'atomistic' device simulator GARAND [9]. Due to purely geometrical effects the drain potential in the FFT controls much smaller fraction of the depletion layer charge under the channel at equivalent doping, dramatically reducing the short channel effects. Therefore, at equivalent subthershold slope (SS) and drain induced barrier lowering (DIBL) the FFT tolerates low channel doping of 5×10^{17}cm^{-3} compared to channel doping of ~1×10^{19} cm^{-3} in its bulk counterpart.

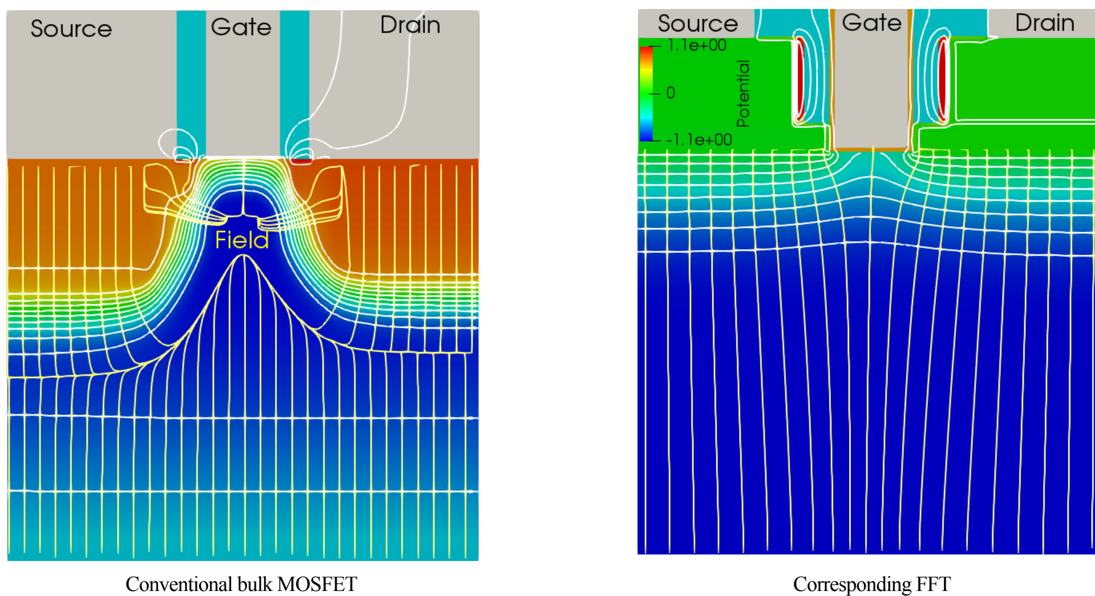


Fig. 1. Comparison between a 20nm Bulk CMOS transistor and the corresponding FFT. Equipotential lines and field lines indicate the potential distributions in the two devices biased at the drain voltage of 50 mV and gate voltage of 0 V.

The FFT concept is applicable to both poly-silicon gate and metal gate bulk CMOS technologies.

3. Performance

Fig. 2 compares the performance of the *n*- and *p*-channel FFTs to the corresponding reference bulk *n*-channel and *p*-channel transistors. For clear comparison the workfunctions of the FFTs are adjusted to deliver the same leakage current of 0.1 µA/µm as in the bulk transistors. The current-voltage (I_D-V_G) characteristics of the reference bulk transistors are calibrated against experimentally reported data [10]. The extracted mobility parameters were used in the simulation of the FFTs.

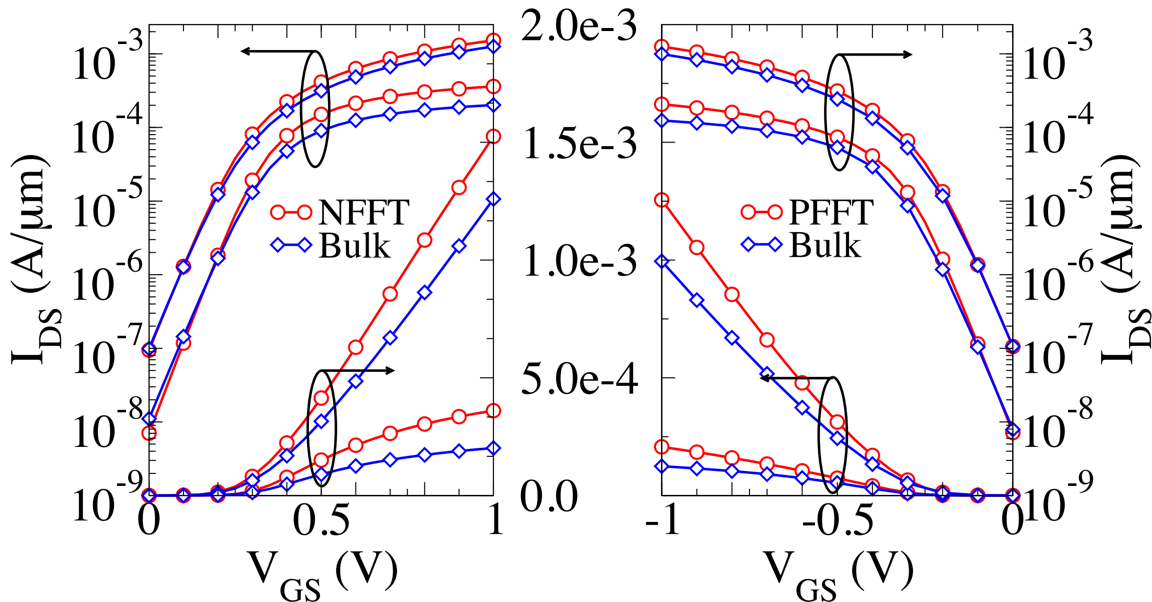


Fig. 2. Comparison of the performance of the *n*- and *p*-channel FFTs to the corresponding reference bulk *n*-channel and *p*-channel transistors

The performance of the FFT in comparison to the reference bulk MOSFET is summarised in Table 1. The drive current improvement at low drain bias for the *n*-channel FFT is 79% and for the *p*-channel FFT is 60%. In 90nm and below bulk CMOS technologies compressive strain is routinely used for increasing the performance of the *p*-channel transistors. It is important to note that the methods used to introduce strain in the reference bulk transistors are fully applicable to the FFTs. In particular, compressive strain is introduced by the formation of sigma shaped carbon rich epitaxial regions, which are in fact easier for implementation in the FFTs [11]. Also, any reduction of the mobility in the carbon-rich regions will have less impact on the FFTs, compared to the reference bulk MOSFETs.

Table 1 FFT and MOSFET performance comparison

Type	V_{DD} *(V)*	FFT I_{on} *(mA/μm)*	Bulk Transisto: I_{on} *(mA/μm)*	Improvement (%)
n	0.05 V	0.36	0.201	79
	1.0 V	1.5	1.2	25
p	0.05 V	0.207	0.129	60
	1.0 V	1.255	0.992	26

At low drain bias the performance of a field effect transistor is proportional to the channel mobility, which dramatically increases in the case of FFT. To qualitatively illustrate the origin of this performance gain in the FFT we refer to Fig. 3, which displays the section of the universal mobility curve [3] that is relevant to this transistor operation. There are two beneficial effects driving a significant mobility increase in the low-doped epitaxial channel transistors. First, the doping reduction lifts the mobility from impurity-scattering dominated values back to the 'universal' mobility curve. Second, reducing the magnitude of the effective vertical electric field results in 'sliding' the mobility in the channel to the left and, therefore, upward along the universal mobility curve. As it can be seen from the figure, easily two-fold increase in mobility can be achieved due to the superposition of the above two effects.

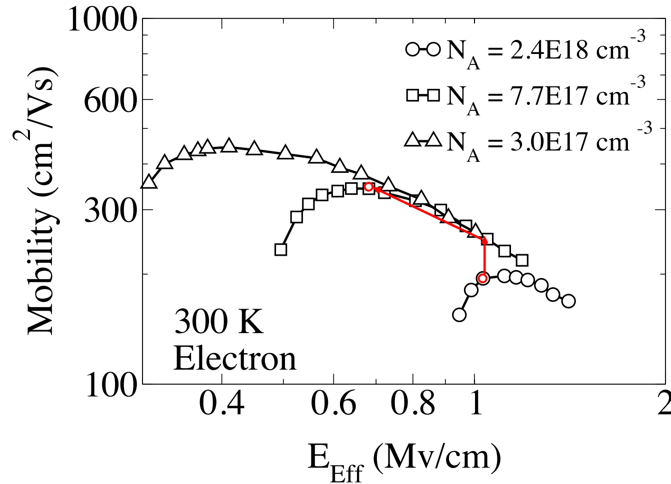


Fig. 3. Impact of doping and vertical field on mobility.

It is well known that low drain voltage performance improvement is proportional to the mobility increase. At high drain bias in contemporary transistors, for example, a 100% improvement in mobility results in less than 50% improvement in the high drain bias conditions when injection velocity dominates the transistor performance [12]. At high drain bias the performance improvement is 25% and 26% for the *n*- and the *p*-channel FFTs respectively. Further analysis shows that about 21% drive current enhancement in the *n*-FFT can be translated into 2 orders of magnitude improvement in the leakage current at equivalent drive current, compared to the reference bulk MOSFET.

The drift-diffusion simulations are reliable when estimating the transistor performance at low drain bias, but they cannot capture non-equilibrium transport effects and are not reliable in predicting the transistor performance at high drain bias.

In this paper, in order to confirm the FFT performance improvements at high drain bias we have conducted ensemble Monte Carlo (EMC) simulations using the EMC module of GARAND [9]. For brevity we will present the results from the *n*-channel FFT only. The *p*-channel results are equally convincing. First, we verify the EMC results against the performance of the reference bulk MOSFETs, bearing in mind that the DD simulations were calibrated against experimental data. Although relatively low level of tensile strain may be present for these devices, introduced for example through tensile nitride layer [13], we do not have the information for the level of strain in the reference transistor and therefore no strain was introduced in the EMC simulations.

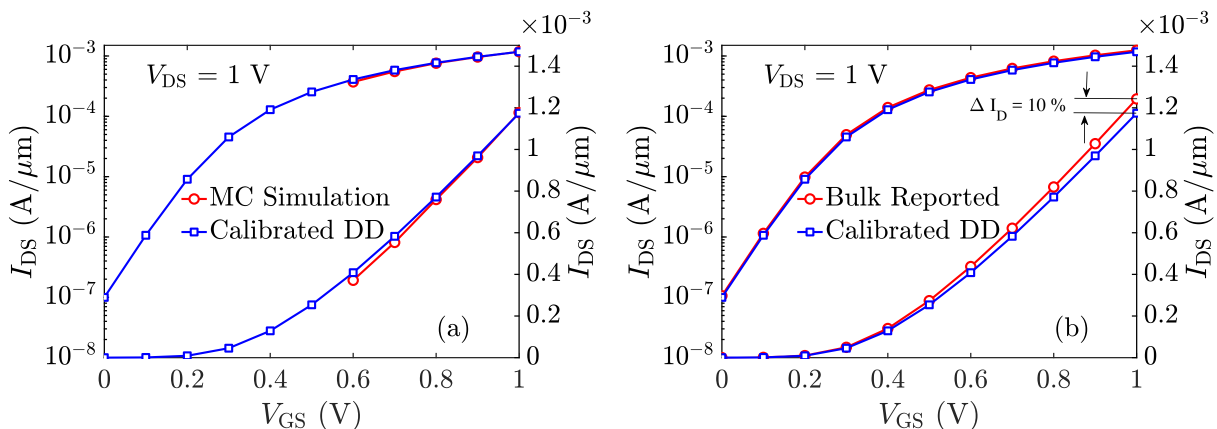


Fig. 4. Fitting of DD to the EMC simulations of the reference bulk transistor (a) and comparison between the experimentally fitted and the EMC fitted DD simulations of the reference bulk transistor (b)

The EMC is noisy and not reliable in the subthreshold region due to the small number of MC particles present in the channel generating significant statistical noise. Therefore, in order to compare the experimental and the simulated results for the reference bulk transistor we first calibrate the DD simulations to the corresponding EMC simulations. The results of the calibration are presented in Fig. 4. (a). The MC calibrated DD simulations were compared to the DD simulation calibrated to the experimental target data in Fig. 4 (b) where workfunction of the EMC simulations is slightly adjusted to deliver the same leakage current of 0.1 μA/μm. There is a good agreement between the reference and the MC simulated I_D-V_G curves with approximately 10% underestimation of the drive current in the MC simulation attributed to the lack of tensile strain.

Similarly, the DD simulations calibrated to the EMC simulations of the FFT were compared to the DD simulations fitted to the EMC simulations of the reference transistor as shown in Fig. 5. The observed 21% improvement in the drive current is in good agreement with the predicted 25% agreement from pure DD simulations.

The slight reduction of the performance improvement in the EMC simulations is due to the lack of strain. Referring to Fig. 3 the lifting of the 'universal' mobility curve in the presence of strain will increase the gain from the shift up from impurity dominated scattering mobility to the surface roughness dominated scattering mobility in presence of strain.

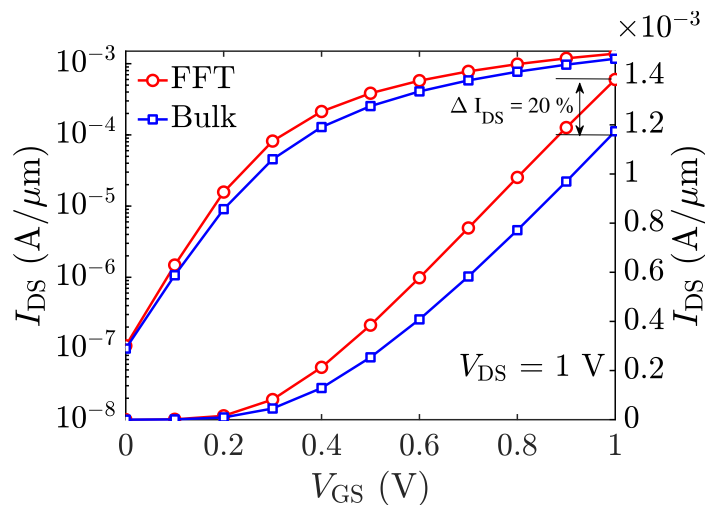


Fig. 5. Comparison of the EMC calibrated DD simulations of the *n*-channel FFT and the reference bulk transistor.

It is well known that the current trajectory of the switching invertors in the integrated circuit never reaches the drive current evaluated V_D=V_G=V_{DD} [14]. A better indicator for the transistor performance is the effective drive current. The effective drive current improvement for the *n*-channel FFT is 34% and for the *p*-channel FFT is 40%.

4. Variability

It is well known that in bulk MOSFETs the random discrete dopants (RDD) induced statistical variability dominate the line edge roughness (LER) induced variability and the poly-silicon gate variability (PSG) or the metal gate granularity (MGG) variability [15]. Therefore, apart from the performance improvement, the reduction in the channel doping concentration of the FFT should result in significant reduction of the short-range purely statistical variability. Simulations of statistical variability were carried out using the DD module of GARAND [9] on statistical samples of 1000 microscopically different transistors. RDD [15] is introduced converting the continuous doping distribution into randomly placed discrete dopants. LER simulation is introduced using a 1-D Fourier synthesis technique with a Gaussian correlated power spectrum with a correlation length of 25 nm and RMS amplitude of 0.66 [16]. In the

MGG [17] simulations we have assumed TiN as a gate material resulting in two work function distributions with probabilities of 40% and 60% [18]. Table 2 compares the short-range (purely statistical) variability in the *n*- and *p*-channel FFTs and the corresponding reference bulk MOSFETs.

Table 2 FFT and MOSFET variability comparison for p-type and n-type devices

		FFT			Bulk		
	V_{DD} [V]	σV_T	C1	Av	σV_T	C1	Av
n	0.05	27	0.68	0.95	57	1.43	2.02
	1.0	33	0.83	1.17	64	1.60	2.26
p	0.05	38	0.95	1.34	65	1.63	2.30
	1.0	43	1.08	1.52	70	1.75	2.47

It is clear that the standard deviation of the threshold voltage (σV_T) of the FFTs at different bias conditions is almost 50% less than the reference bulk MOSFET. This can result in significant reduction of the supply voltage and the minimum holding voltage (V_{min}) of the corresponding SRAM arrays and in significant increase of the SRAM yield.

The reduction of σV_T also results in significant reduction in the leakage current of the FFTs at equivalent threshold voltage due to the log-normal distribution of the leakage current. Bearing in mind that $\sigma \log_{10}(I_D) = \sigma V_T / SS$, a twofold reduction of σV_T at SS~100 mV/dec results in 3 times reduction of the average leakage current in the FFT compared to the reference bulk transistor. Together with the gain in leakage current resulting from the performance improvement, this accumulates to almost two orders of magnitude (1.8) leakage current reduction at identical drive current, compared to the reference bulk transistor. This translates to almost two orders of magnitude increase of the standby battery life in IoT applications.

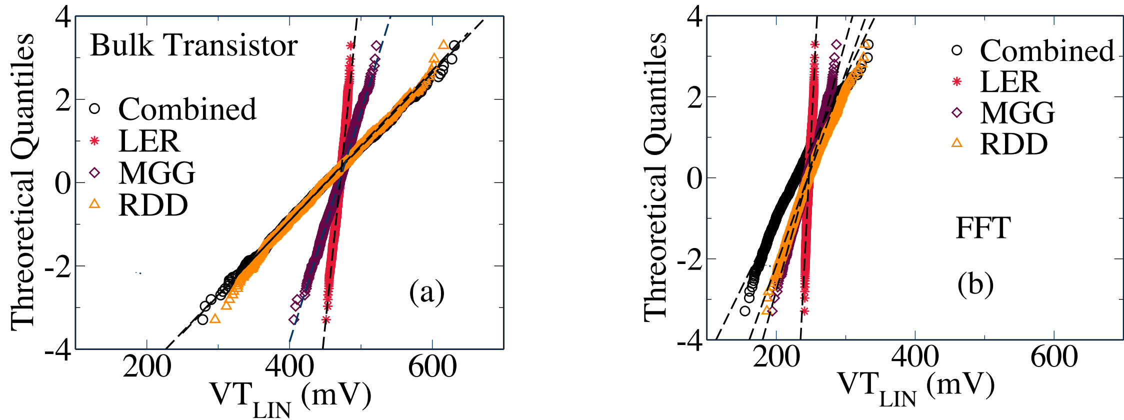


Fig. 6. Threshold voltage distributions associated with the individual and combined sources of statistical variability at low drain bias of 50 mV in both conventional transistor (left) and FFT transistor (right).

In order to understand the individual contributions of the statistical variability sources we have conducted simulation of the individual and combined impact of RDD, LER and MGG on the variability of the FFT and the reference bulk MOSFET. Due to lack of space, only data for the *n*-channel transistors are presented. Fig. 6 presents the corresponding threshold voltage distributions.

Table 3 FFT and MOSFET variability comparison. C1, Av [mV-µm] are calculated using σ_{VTLIN} at V_D=50 mV

	FFT			Bulk		
Variability	σ_{VT}	C1	Av	σ_{VT}	C1	Av
RDD	22	0.55	0.78	54	1.35	1.91
MGG	15	0.38	0.53	17	0.43	0.60
LER	3	0.08	0.11	6	0.15	0.21
Combined	27	0.68	0.95	57	1.43	2.02

The p-channel data are qualitatively identical. Table 3 compares the impact of each source of statistical variability on the n- and p-channel FFTs and the corresponding reference bulk MOSFETs.

It is important to understand until what doping concentration in the channel, the FFT will remain superior to the reference bulk MOSFET in terms of statistical variability and performance. Table 4 shows the threshold voltage standard deviation for FFTs with different channel doping concentrations. It is expected that the variability increases with increasing channel doping as shown in Table 4. However even at the highest channel doping level of 1×10^{18}cm^{-3} the FFT exhibits significantly low variability when compared with the conventional bulk transistor, which has σV_T= 57 mV at the drain bias of V_D = 0.05 V and 64 mV at V_D = 1.0 V (at a peak channel doping of ~2×10^{19} cm^{-3} in the bulk transistor).

Table 4 FFT variability as a function of the channel doping. C1, Av are calculated using σ_{VTLIN} at low V_D=50 mV

Concentration [cm^{-3}]	σ_{VTLIN} [mV]	V_{TSAT} [mV]	C1 mV-µm	Av mV-µm
5×10^{17}	28	33	0.70	0.99
1×10^{18}	32	37	0.89	1.13
1.5×10^{18}	36	42	0.9	1.27
2×10^{18}	39	43	0.98	1.38
Bulk	57	64	1.43	2.02

Table 5 compares the ON-current at high drain (1 V) and low drain (50 mV) biases. As expected, the performance is degraded as a result of introduction of higher channel doping. Although the percentage I_{ON} difference between the transistors, which are doped with $N_A = 5\times10^{17}$ cm^{-3} and $N_A = 1\times10^{18}$ cm^{-3} is minimal (~1%), there is a significant performance degradation between 5×10^{17} cm^{-3} and 2×10^{18} cm^{-3} (~13.5%). The performance degradation at low drain bias is much larger. Still the FFT performance remains significantly higher than the performance of the reference bulk MOSFET.

Table 5 Performance as a function of the channel doping. The percentage improvement of derive current of FFT over the conventional bulk transistor is calculated by aligning the leakage current to I_{OFF}=1nA/µm.

Concentration [cm^{-3}]	I_{ON-LIN} [mA/µm]	I_{ON-SAT} [mA/µm]	I_{ON-SAT} Improvement [%]
5×10^{17}	0.312	1.25	21
1×10^{18}	0.258	1.130	12
1.5×10^{18}	0.223	1.054	6.1
2×10^{18}	0.198	0.990	-
Bulk MOSFET	0.16	0.992	-

Fig. 7 compares the amplitude of random telegraph signal (RTS) in the FFT and the reference bulk transistor. It is clear that the RTS amplitudes in the FFT transistor are approximately 3 times lower compared to the reference bulk transistor. This will reduce the jitter and will significantly improve the yield of the corresponding SRAM arrays. Bearing in mind that the Low Noise (LN) power spectrum is directly proportional to σI_D^2 distribution and in turn σI_D is proportional to σV_T. Simulations show that the FFTs will have one order of magnitude lower LN power spectrum compared to the reference bulk transistors.

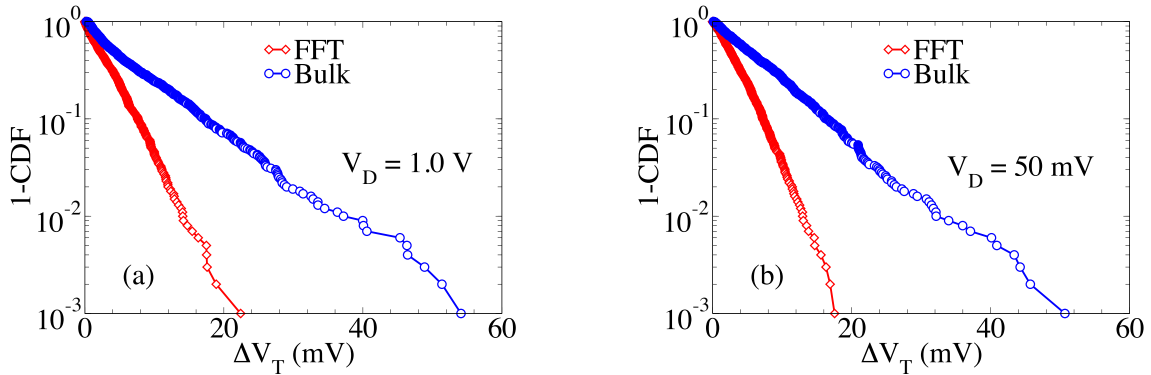


Fig. 7. Comparison of the RTS amplitudes distribution in the FFT with the reference bulk MOSFET at high (a) and low (b) drain bias conditions.

Fig. 8 compares the RTS amplitudes distribution in the FFTs with different doping in the technologically important region and in the reference bulk transistor. The distributions are obtained from a statistical sample of 1000 atomistically different transistors with random position of the RTS trap.

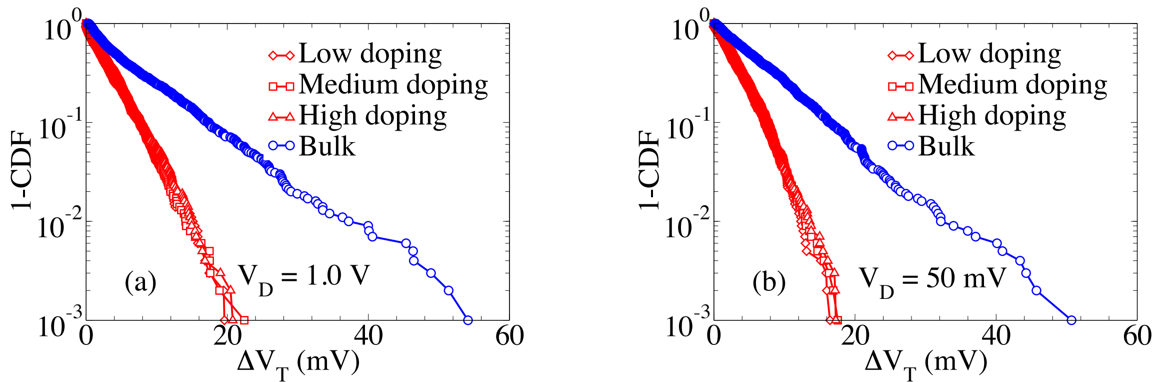


Fig. 8. RTS amplitudes distribution in the FFTs with different doping in the technologically important region and in the reference bulk MOSFET, at high (a) and low (b) drain bias conditions.

5. Circuit Performance

We compare the circuit performance of the FFTs in relation to the reference bulk MOSFETs. Two types of metrics are usually used to evaluate the digital performance of a particular technology – the speed evaluated using ring oscillator (RO) simulations and the SRAM performance usually focusing on the minimum supply voltage that guaranties the yield of particular size SRAM array.

In order to access the circuit performance, we have first extracted the compact model parameters using TCAD generated target I-V and C-V characteristics for the *n*- and *p*- channel FFTs and the corresponding reference bulk transistors. Accurate nominal uniform BISIM4 compact models were extracted using the Synopsys compact model extractor Mystic [9]. The long-range process variability was simulated by introducing realistic threshold voltage shift for the slow (SS), fast (FF) and mixed corners (SF, FS). Statistical TCAD simulations were used to generate the statistical characteristics for capturing the local variability in BSIM4 using the methodology described in [19].

It could be speculated that the increased parasitic gate capacitances associate with the gate facing particularly the first epitaxial layer, can reduce the performance improvement benefits of the FFT. In order to compare the realistic circuit performance, we have simulated a 7-stage RO with a fan-out of three where each stage consists of three inverters as shown in Fig. 9 (a). The width

of the transistors was W=7L. Simple RC interconnect model with lumped capacitance C and resistance R were used in the simulations. The values of R and C were evaluated from realistic level 2/3 interconnects typical for the 20 nm bulk CMOS technology generation.

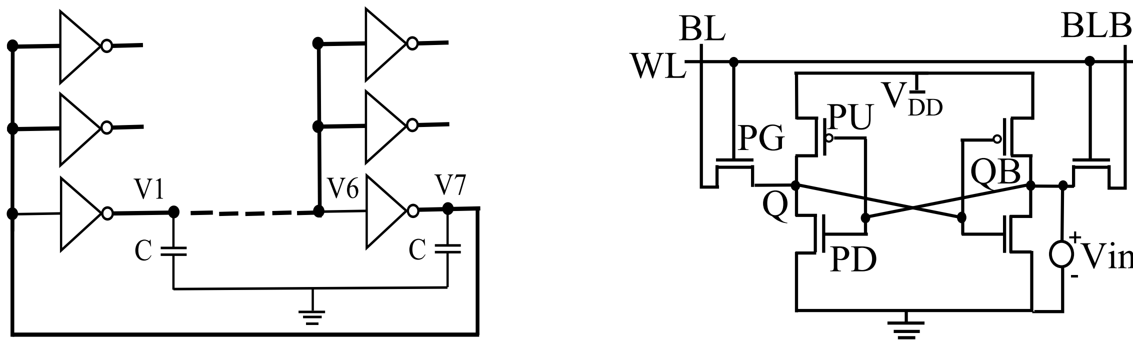
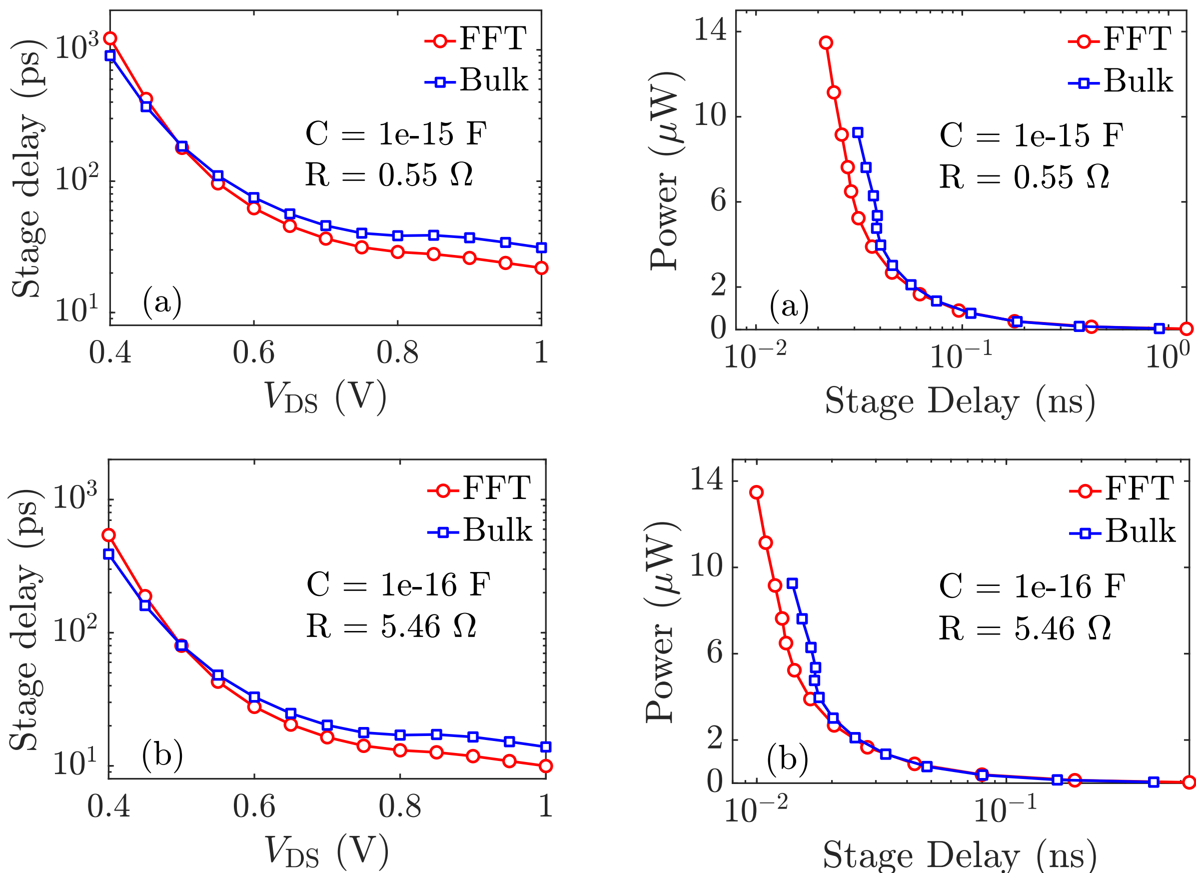


Fig. 9 (a) 7-stage RO with a fan-out of three. (b) Schematic of a 6-T SRAM cell including the arrangement for *n*-curve measurement. PU: Pull Up, PD: Pull Down, PG: Pass Gate transistors, BL/BLB: Bit/BitBar line, WL: Word line, VDD: Supply Voltage, Q/QB are the storage nodes. N-curve measurement: The *n*-curves for read and write conditions are obtained by plotting the applied voltage V_{in} (sweeped from 0 V to V_{DD}) at "0" internal storage node (QB) against the current I_{in} while the bit lines and word lines are maintained at appropriate voltages.

Three sets of simulations were carried out assuming short ($C=10^{-17}$ F, R=0.55 Ω), medium ($C=10^{-16}$ F, R=5.5 Ω) and long range interconnects ($C=10^{-15}$ F, R=55 Ω). The corresponding stage delay times for the FFTs and their bulk counterparts are compared in Fig. 10 in the case of the three different interconnect scenarios. The stage delays of the FFT ROs become shorter for supply voltages above 0.5V. The performance improvement in the FFT case increases further with with the supply voltage reaching 25% reduction in the stage delay at supply voltage of 1V.



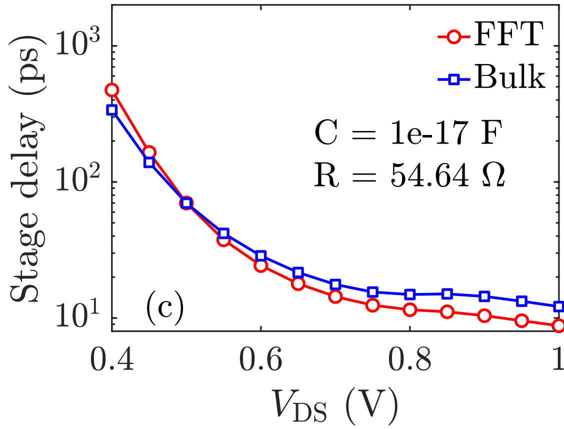


Fig. 10 Stage delay time of RO as a function of supply voltage for (a) short, (b) medium, and (c) long interconnects.

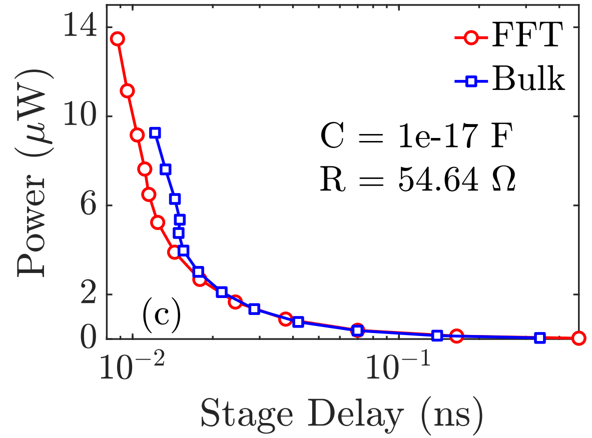


Fig. 11 Power dessipation as a function of stage delay time of RO for (a) short, (b) medium, and (c) long interconnects.

It is instructive to analyse also the dependence of the RO power dissiparion as a function of the stage delay for the three interconnect scenarios compared in Fig. 11. At stage delay times below 100 ps the power dissipation of the FFF ROs becomes smaller than the power dissipation of the bulk MOSFET ROs. This difference increases with the reduction of the stage delay time. At stage delay time of 30 ps the FFT ROs consume less than half of the power of the bulk MOSFET ROs.

We also compared the performance of 6-T SRAM cells designed using the FFT and the conventional reference 20nm CMOS bulk MOSFET. The Pull-Up (PU), Pass-Gate (PG) and Pull-Down transistor widths have been set to a ratio of 1:2:3. We have focused on the evaluation of the read stability and write ability in terms of the critical currents under read and write conditions obtained from the analysis of the respective *n*-curves [19]. We also present the results for the minimum supply voltage (V_{min}) of the SRAMs.

The schematic of the 6-T SRAM cell including the setup for extracting the *n*-curves is shown in Figure 9(b). Icrit (critical read stability current is the minimum current needed to cause a destructive read and is given by the peak current in the read n-curve. Icritw (critical write ability current) is given by the minimum of the valley in the write *n*-curve. It must be positive for a successful write operation.

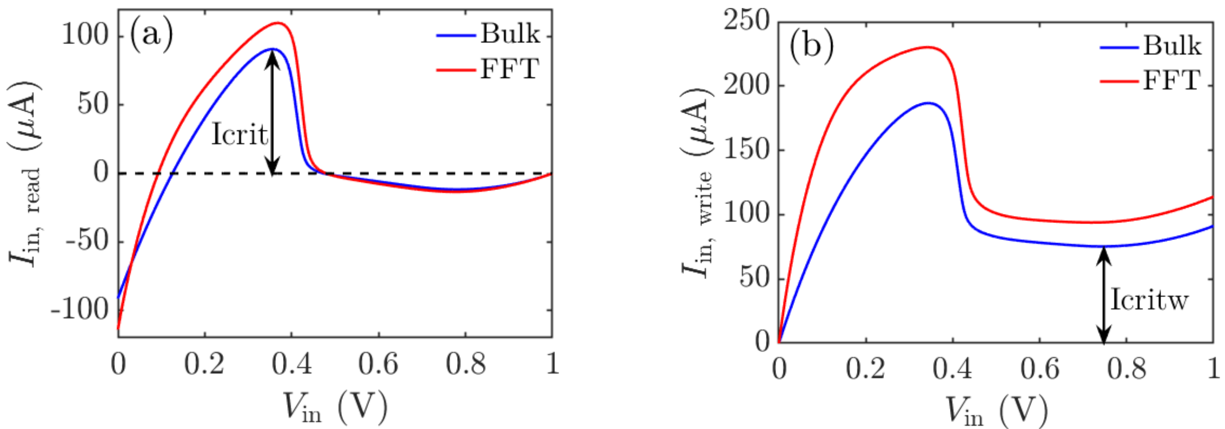


Fig. 12. Comparison of the nominal n-curves for bulk and FFT based SRAM for (a) Read, and (b) Write conditions. Also shown are the definitions of Icrit and Icritw. Both the metrics are higher for FFT based SRAM than the bulk CMOS based SRAM. V_{DD} = 1V.

The read and write n-curves for the nominal SRAM cell are illustrated in Fig. 12. We find that the FFT based SRAM cell displays higher Icrit under READ condition as well as higher I_{critw} under WRITE condition. To explore the impact of variability, we performed statistical Monte Carlo simulations with 1000 samples for the 6T SRAM. Probability distribution of I_{crit} and I_{critw} are shown in Fig. 13. These results demonstrate the improvement in the magnitude and reduction of the statistical spread of the SRAM metrics.

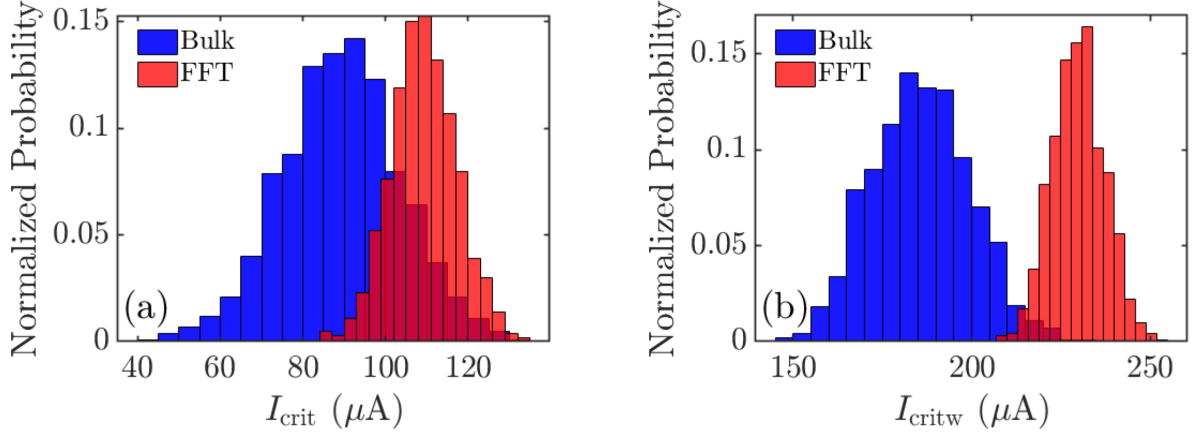


Fig. 13. Histograms showing the probability distributions of (a) Icrit from Read n-curves, and (b) Icritw from Write n-curves corresponding to the statistical simulations. It is evident that the FFT based SRAMs have lesser variability in the critical currents while having higher mean value. V_{DD} = 1V.

The minimum supply voltage required for reliable operation, V_{min} in SRAMs is critically constrained by variability, and hence FFTs due to their variability resistance are expected to offer reduced V_{min} compared to their bulk counterparts. Indeed, we find that FFT based SRAM shows much better V_{min} than bulk SRAM as illustrated in Fig. 14. The improvement in V_{min} is around 30% with respect to both Icrit and Icritw for the typical corner.

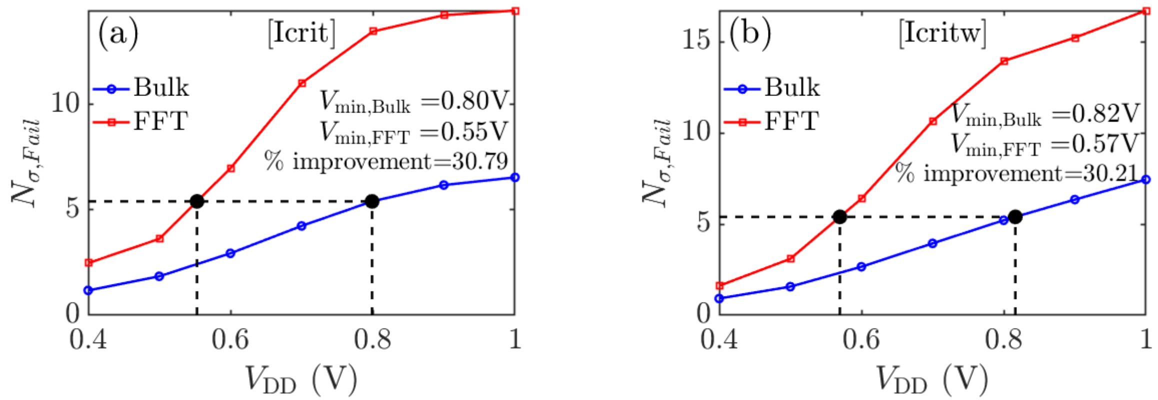


Fig. 14. V_{min} calculation considering critical currents (a) Icrit, and (b) Icritw. We calculate $N_{\sigma,Fail}$ as V_{DD} is varied. $N_{\sigma,Fail} = \mu/\sigma$, where μ and σ are the mean value and standard deviation of Icrit and Icritw obtained from 1000 Monte-Carlo runs in the circuit simulator. A target $N_{\sigma,Fail}$ is then set. The V_{DD} corresponding to the target $N_{\sigma,Fail}$ is the V_{min}. In this work we have set the target $N_{\sigma,Fail}$ to 5.4.

6. Conclusions

In this white paper we evaluated the transistor performance and circuit performance of a novel Flat Field Transistor (FFT) in comparison with a conventional bulk MOSFET both designed to meet the requirements of the 20nm bulk CMOS technology generation. At transistor level the FFT outperforms the bulk MOSFET by more than 20% at 1V supply voltage. The performance

improvement increases with the reduction of the supply voltage. Despite somewhat increase gate capacitance the FFT ROs have shorter stage delay for supply voltages above 0.5V with the delay improvement increasing with the supply voltage to more than 20% at V_{DD}=1V. More importantly the overall RO power dissipation in the FFT case is less than 50% of the bulk power dissipation and delays smaller than 30ps. We also demonstrate that the FFT based SRAM offers better read stability and write ability and a V_{min} reduction by around 30%.

. References

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